Sai Govardhan

CONTACT
INFORMATION

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EDUCATION

B.Tech in Electronics and Communication Engineering   2019 - 2023
PES University, Bangalore

- VLSI Specialization
- Thesis: Low Power Multidimensional Hardware Sorting Accelerator
    Advisor: Dr. Sudeendra Kumar K.

EXPERIENCE

Microarchitect   June 2025 - Present
Agrani Labs, Bangalore
- Currently in Stealth Mode

CPU Design Engineer - II   Nov 2023 - June 2025
InCore Semiconductors, Bangalore
- MultiCore Cache Subsystem Microarchitect (Sept 2024 - June 2025)
    Mid Level and Last Level Cache Microarchitecture and RTL Design
    Tilelink to AXI4 Bridge RTL Design
    Bluecheck based Unit Level Test Setup
    Advisors: Niraj Sharma and Gautam Doshi
- In-Tst-1 SoC Tapeout Contributor (Jan 2024 - Aug 2024)
    Azurite + Calcite SoC on TSMC 40LP - ***silicon proven***
    Linting, CDC, Synthesis and LEC
    IO-PAD and PinMux Integration
    SRAM and ROM Generation and Integration
    PinMux uArch and BSV Generator Design
    Advisor: Arjun Menon and Niraj Sharma
- RISC-V CPU Extecution Cluster Retiming (July - Nov 2023)
    Integer, Multiply/Divide, Floating Point, Bit-Manip and Packed-SIMD
    Advisors: Babu P.S. and Neel Gala

VLSI Design Intern   Jan 2023 – June 2023
International Institute of Information Technology, Bangalore
- Ganaka Architecture Performance Intern
    Memory Subsytem Performance Modeling using SPEC CPU 2017
    Dr. G. N. Srinivasa Prasanna

Hardware Accelerator Research Intern   Jan 2023 – June 2023
Centre for Innovation and Entrepreneurship, PES University
- Implementation of Architectures for Hardware Acceleration on the Intel Cyclone DE10 FPGA
- FPGA Track Lead for the CIE Summer Workshop 2023
    Prof. Sathya Prasad

Electronics Research Intern   Sept 2022 – Dec 2022
OrbitAID Aerospace, Indian Institute of Science, Bangalore

- Research topic: On Orbit Servicing of Space System Architectures
  Advisor: Sakthikumar R.

TEACHING

Embedded Firmware Development with UEFI [GitHub Link]
Student Teaching Assistant, PES University
- Demonstration of the UEFI shell basics on QEMU using TianoCore's EDKII platform.
  Advisor: Dr. Sudeendra Kumar K.

Synthesis, Physical Design and Timing Analysis of Digital Circuits [Manual]
Student Teaching Assistant, PES University
- Implementation of RTL to Floorplan demos on the Mentor Oasys tool, and analysis of physical design characteristics and timing analysis.
  Advisor: Dr. Sudeendra Kumar K.

Digital System Design [GitHub Link] [Manual]
Student Teaching Assistant, PES University
- Hands-on Advanced Digital Design Projects on Cadence Tools from RTL to GDSII, for 190+ students.
  Advisor: Dr. Rashmi Seethur

PUBLICATIONS

Low Power Multidimensional Sorters using Clock Gating and Index Sorting
Samahith S A, **Sai Govardhan**, *Manogna R, Hitesh D, Dr. Sudeendra Kumar K*
Nominated for the best paper award in the IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT), July 2023. [Paper Link]

SKILLS

Digital Design: RTL Linting and CDC, Synthesis, Static Timing Analysis, Logical Equivalence Checking, Gate Level Simulation, SRAM and ROM generation
Computer Architecture: RISC-V ISA implementation, Cache Coherence
CPU Benchmarking: SPEC CPU 2017
Verification: Functional and Formal Verification (Assertions)
Hardware Description Languages: Bluespec SystemVerilog, Verilog
Imperative Programming Languages: C, C++
Scripting Languages: Python, TCL and Bash
Electronic Design Automation Tools:
Cadence (Xcelium, Genus, Conformal LEC, Tempus, Incisive Metrics Center),
Synopsys(Spyglass), Mentor(QuestaSim, Oasys), Xilinx(Vivado), Intel(Quartus Prime),
TSMC(Memory Compilers), Verilator

WORKSHOPS

CIE Summer Workshop   March 2023 - June 2023
PES University, RR Campus, Bangalore
Was the FPGA Track lead of the CIE Summer workshop, which involved guiding four teams for four weeks on the fundamentals of mapping and implementing algorithms to hardware architectures on the Intel DE-10 FPGA Board. **[GitHub Link]**

CIOT Workshop   October 2021
PES University, RR Campus, Bangalore
Presented the Farmbot project in which I was the electronics lead, and trained students with IOT fundamentals using dev-kits for two days. **[GitHub Link]**

CERTIFICATIONS	**Advanced Computer Architecture** *NPTEL Online Certification* [**Certificate Link**]
	Genus Synthesis Solution with Stylus Common UI v21.1 *Cadence Digital Badge Programme* [**Credly Link**]
	Low-Power Synthesis Flow with Genus Stylus Common UI v21.1 *Cadence Digital Badge Programme* [**Credly Link**]
	Conformal Equivalence Checking v22.1 *Cadence Digital Badge Programme* [**Credly Link**]
	Basic Static Timing Analysis v2.0 *Cadence Digital Badge Programme* [**Credly Link**]
	Tempus Signoff Timing Analysis and Closure v21.1 *Cadence Digital Badge Programme* [**Credly Link**]
	Fundamentals of IEEE 1801 Low-Power Specification Format v8.0 *Cadence Digital Badge Programme* [**Credly Link**]
	Cadence RTL-to-GDSII Flow v4.0 *Cadence Digital Badge Programme* [**Credly Link**]
	Joules Power Calculator v21.1 *Cadence Digital Badge Programme* [**Credly Link**]
AWARDS	**Won the Certificate of Appreciation** *Was one of the few recipients of the appreciation award for the graduating batch of BTech ECE at PES University, for my contributions to the VLSI Domain*
	Won 2nd place at the Hackezee Hackathon *For the IoT and sensors project- 'Gesture Controlled Rescue Vehicle' in the flagship hackathon organized by the ECE Department PESU*
	Won 3rd place at the Gutsy Entrepreneur 2.0 Contest *For the EmoBuild (Emotional Intelligence - Build Platform) business idea and prototype app design at the 14-day hackathon organized by CIE PESU*
	Won 2nd place at Pioneer *The Business Modelling Contest, by presenting creative strategies for existing businesses navigating the pandemic, in an event organized by CIE PESU*
	Distinction Awards for the I, II, V and VI semesters *by the ECE Department, PES University*
	Won the Most Disciplined Outgoing Student award *at Presidency School, Nandini Layout*