Xilinx Condensed Applicability Table

Family/Device	Unit Cost ($)	Needs PHY	# 10 GbE	Expandability(1)	Normalized Logic Cells
Spartan 6					
XC6SLX45T-3CSG324T	**69**	**Y**	**1**	**N**	**1**
XC6SLX45T-3FG484T	**79**	**Y**	**1**	**Y**	**1**
XC6LSX75T-3 FG676	**147**	**Y**	**2**	**Y**	**1.7**
Artix					
XC7A20SLT-2CSG326	**(avail?)**	**Y**	**1**	**Y**	**0.37**
XC7A35SLT-2CSG326	**(avail?)**	**Y**	**1**	**Y**	**0.75**
XC7A50SLT-2FGG677	**(avail?)**	**Y**	**1**	**Y**	**1.2**
XC7A100LT-2FGG676	**210**	**Y**	**2**	**?**	**2.3**
Kintex					
XC7K70T-2FBG676	**183**	**N**	**2**	**Y**	**1.5**
XC7K160T-3FFG676	**460 (avail?)**	**N**	**2**	**Y**	**3.7**
Zync					
XC7Z030-3FBG676E	**409 (100)**	**N**	**1**	**Y**	**2.9**
XC7Z045- 1FBG676C	**1542**	**N**	**2**	**N**	**8**

Notes
1 – Expandability means that there are bigger FPGAs in the same package

Discussion:

Best bet for single 10 GbE link is XC6SLX45T-3FG484T. It costs $10 more than the smallest Spartan but is expandable.

However, the XC7K70T-2FBG676 is about equivalent when you subtract the price of the PHY. It gets even more competitive if you factor in the cost of the board itself and would save a bit of power.

The Zyncs are not competitive when you subtract out the costs of the PHY and processor (409 – 90 – 90 = $229), but they are not that far off.

Family Condensed Feature Summary

Table 1: **Spartan-6 FPGA Feature Summary by Device**

Device	Logic Cells[1]	Configurable Logic Blocks (CLBs)			DSP48A1 Slices[3]	Block RAM Blocks		CMTs[5]	Memory Controller Blocks (Max)[6]	Endpoint Blocks for PCI Express	Maximum GTP Transceivers	Total I/O Banks	Max User I/O
		Slices[2]	Flip-Flops	Max Distributed RAM (Kb)		18 Kb[4]	Max (Kb)						
XC6SLX4	3,840	600	4,800	75	8	12	216	2	0	0	0	4	132
XC6SLX9	9,152	1,430	11,440	90	16	32	576	2	2	0	0	4	200
XC6SLX16	14,579	2,278	18,224	136	32	32	576	2	2	0	0	4	232
XC6SLX25	24,051	3,758	30,064	229	38	52	936	2	2	0	0	4	266
XC6SLX45	43,661	6,822	54,576	401	58	116	2,088	4	2	0	0	4	358
XC6SLX75	74,637	11,662	93,296	692	132	172	3,096	6	4	0	0	6	408
XC6SLX100	101,261	15,822	126,576	976	180	268	4,824	6	4	0	0	6	480
XC6SLX150	147,443	23,038	184,304	1,355	180	268	4,824	6	4	0	0	6	576
XC6SLX25T	24,051	3,758	30,064	229	38	52	936	2	2	1	2	4	250
XC6SLX45T	43,661	6,822	54,576	401	58	116	2,088	4	2	1	4	4	296
XC6SLX75T	74,637	11,662	93,296	692	132	172	3,096	6	4	1	8	6	348
XC6SLX100T	101,261	15,822	126,576	976	180	268	4,824	6	4	1	8	6	498
XC6SLX150T	147,443	23,038	184,304	1,355	180	268	4,824	6	4	1	8	6	540

Table 2: **Spartan-6 Device-Package Combinations and Maximum Available I/Os**

Package	CPG196[1]	TQG144[1]	CSG225[2]	FT(G)256[3]	CSG324		FG(G)484[3,4]		CSG484[4]		FG(G)676[3]		FG(G)900[3]	
Body Size (mm)	8 x 8	20 x 20	13 x 13	17 x 17	15 x 15		23 x 23		19 x 19		27 x 27		31 x 31	
Pitch (mm)	0.5	0.5	0.8	1.0	0.8		1.0		0.8		1.0		1.0	
Device	User I/O	User I/O	User I/O	User I/O	GTPs	User I/O	GTPs	User I/O	GTPs	User I/O	GTPs	User I/O	GTPs	User I/O
XC6SLX4	106	102	132											
XC6SLX9	106	102	160	186	NA	200								
XC6SLX16	106		160	186	NA	232								
XC6SLX25				186	NA	226	NA	266						
XC6SLX45					NA	218	NA	316	NA	320	NA	358		
XC6SLX75							NA	280	NA	328	NA	408		
XC6SLX100							NA	326	NA	338	NA	480		
XC6SLX150							NA	338	NA	338	NA	498	NA	576
XC6SLX25T					2	190	2	250						
XC6SLX45T					4	190	4	296	4	296				
XC6SLX75T							4	268	4	292	8	348		
XC6SLX100T							4	296	4	296	8	376	8	498
XC6SLX150T							4	296	4	296	8	396	8	540

Table 2: **Artix-7 FPGA Feature Summary by Device**

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP48E1 Slices[2]	Block RAM Blocks[3]			Clock Mgmt Tiles (CMTs)[4]	PCIe[5]	GTPs	XADC Blocks[6]	Total I/O Banks[7]	Max User I/O[8]
		Slices[1]	Max Distributed RAM (Kb)		18Kb	36Kb	Max (Kb)						
XC7A20SL	16,000	2,500	208	60	60	30	1,080	3	0	0	1	5	216
XC7A35SL	32,909	5,142	453	120	130	65	2,340	3	0	0	1	5	216
XC7A50SL	52,480	8,200	688	180	190	95	3,420	4	0	0	1	6	300
XC7A75SL	71,642	11,194	974	240	250	125	4,500	4	0	0	1	6	300
XC7A20SLT	16,000	2,500	208	60	60	30	1,080	3	1	4	1	5	216
XC7A35SLT	32,909	5,142	453	120	130	65	2,340	3	1	4	1	5	216
XC7A50SLT	52,480	8,200	688	180	190	95	3,420	4	1	8	1	6	300
XC7A75SLT	71,642	11,194	974	240	250	125	4,500	4	1	8	1	6	300
XC7A100T	101,440	15,850	1,188	240	270	135	4,860	6	1	8	1	6	300
XC7A200T	215,360	33,650	2,888	740	730	365	13,140	10	1	16	1	10	500

Table 3: **Artix-7 FPGA Device-Package Combinations and Maximum I/Os**

Package[1]	CPG236			CSG325			CSG484			CPG237			CSG326			CSG485			FGG677		
Size (mm)	10 x 10			15 x 15			19 x 19			10 x 10			15 x 15			19 x 19			27 x 27		
Ball Pitch (mm)	0.5			0.8			0.8			0.5			0.8			0.8			1.0		
Device	GTP	I/O		GTP	I/O		GTP	I/O		GTP	I/O		GTP	I/O		GTP	I/O		GTP	I/O	
		HR[2]	HD[3]		HR[2]	HD[3]		HR[2]	HD[3]		HR[2]	HD[3]		HR[2]	HD[3]		HR[2]	HD[3]		HR[2]	HD[3]
XC7A20SL	0	48	52	0	108	108															
XC7A35SL	0	48	52	0	108	108															
XC7A50SL							0	144	156												
XC7A75SL							0	144	156												
XC7A20SLT										1	48	52	4	108	77	4	108	108			
XC7A35SLT										1	48	52	4	108	77	4	108	108			
XC7A50SLT													4	108	77	6	126	108	8	144	156
XC7A75SLT													4	108	77	6	126	108	8	144	156

Table 5: **Kintex-7 FPGA Feature Summary by Device**

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP Slices[2]	Block RAM Blocks[3]			CMTs[4]	PCIe[5]	GTXs	XADC Blocks	Total I/O Banks[6]	Max User I/O[7]
		Slices[1]	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)						
XC7K70T	65,600	10,250	838	240	270	135	4,860	6	1	8	1	6	300
XC7K160T	162,240	25,350	2,188	600	650	325	11,700	8	1	8	1	8	400
XC7K325T	326,080	50,950	4,000	840	890	445	16,020	10	1	16	1	10	500
XC7K355T	356,160	55,650	5,088	1,440	1,430	715	25,740	6	1	24	1	6	300
XC7K410T	406,720	63,550	5,663	1,540	1,590	795	28,620	10	1	16	1	10	500
XC7K420T	416,960	65,150	5,938	1,680	1,670	835	30,060	8	1	32	1	8	400
XC7K480T	477,760	74,650	6,788	1,920	1,910	955	34,380	8	1	32	1	8	400

Table 6: **Kintex-7 FPGA Device-Package Combinations and Maximum I/Os**

Package[1]	FBG484			FBG676[2]			FFG676[2]			FBG900[3]			FFG900[3]			FFG901			FFG1156		
Size (mm)	23 x 23			27 x 27			27 x 27			31 x 31			31 x 31			31 x 31			35 x 35		
Ball Pitch (mm)	1.0			1.0			1.0			1.0			1.0			1.0			1.0		
Device	GTX	I/O		GTX	I/O		GTX	I/O		GTX	I/O		GTX	I/O		GTX	I/O		GTX	I/O	
		HR[4]	HP[5]		HR[4]	HP[5]		HR[4]	HP[5]		HR[4]	HP[5]		HR[4]	HP[5]		HR[4]	HP[5]		HR[4]	HP[5]
XC7K70T	4	185	100	8	200	100															
XC7K160T	4	185	100	8	250	150	8	250	150												
XC7K325T				8	250	150	8	250	150	16	350	150	16	350	150						
XC7K355T																24	300	0			
XC7K410T				8	250	150	8	250	150	16	350	150	16	350	150						
XC7K420T																28	380	0	32	400	0
XC7K480T																28	380	0	32	400	0

Table 1: **Zynq-7000 All Programmable SoC *(Cont'd)***

	Zynq-7000 All Programmable SoC				
	Device Name	Z-7010	Z-7020	Z-7030	Z-7045
	Part Number	XC7Z010	XC7Z020	XC7Z030	XC7Z045
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix™-7 FPGA	Artix-7 FPGA	Kintex™-7 FPGA	Kintex-7 FPGA
	Programmable Logic Cells (Approximate ASIC Gates[3])	28K Logic Cells (~430K)	85K Logic Cells (~1.3M)	125K Logic Cells (~1.9M)	350K Logic Cells (~5.2M)
	Look-Up Tables (LUTs)	17,600	53,200	78,600	218,600
	Flip-Flops	35,200	106,400	157,200	437,200
	Extensible Block RAM (# 36 Kb Blocks)	240 KB (60)	560 KB (140)	1,060 KB (265)	2,180 KB (545)
	Programmable DSP Slices (18x25 MACCs)	80	220	400	900
	Peak DSP Performance (Symmetric FIR)	100 GMACs	276 GMACs	593 GMACs	1,334 GMACs
	PCI Express® (Root Complex or Endpoint)	—	—	Gen2 x4	Gen2 x8
	Agile Mixed Signal (AMS) / XADC	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs			
	Security[2]	AES and SHA 256b for Boot Code and Programmable Logic Configuration, Decryption, and Authentication			

Table 2: **Device-Package Combinations: Maximum I/Os and GTX Transceivers**

Package[1]	CLG225				CLG400				CLG484				FBG484				FBG676				FFG676				FFG900			
Size	13 x 13 mm				17 x 17 mm				19 x 19 mm				23 x 23 mm				27 x 27 mm				27 x 27 mm				31 x 31 mm			
Ball Pitch	0.8 mm				0.8 mm				0.8 mm				1.0 mm				1.0 mm				1.0 mm				1.0 mm			
Transceiver Speed													6.6 Gb/s				6.6 Gb/s				12.5 Gb/s				12.5 Gb/s			
Device	PS I/O	GTX	Select I/O		PS I/O	GTX	Select I/O		PS I/O	GTX	SelectIO		PS I/O	GTX	SelectIO		PS I/O	GTX	SelectIO		PS I/O	GTX	SelectIO		PS I/O	GTX	SelectIO	
			HR[2]	HP[3]			HR[2]	HP[3]			HR[2]	HP[3]			HR[2]	HP[3]			HR[2]	HP[3]			HR[2]	HP[3]			HR[2]	HP[3]
XC7Z010	86	0	54	–	130	0	100	–																				
XC7Z020					130	0	125	–	130	0	200	–																
XC7Z030													130	4	100	63	130	4	100	150	130	4	100	150				
XC7Z045																	130	8	100	150	130	8	100	150	130	16	212	150

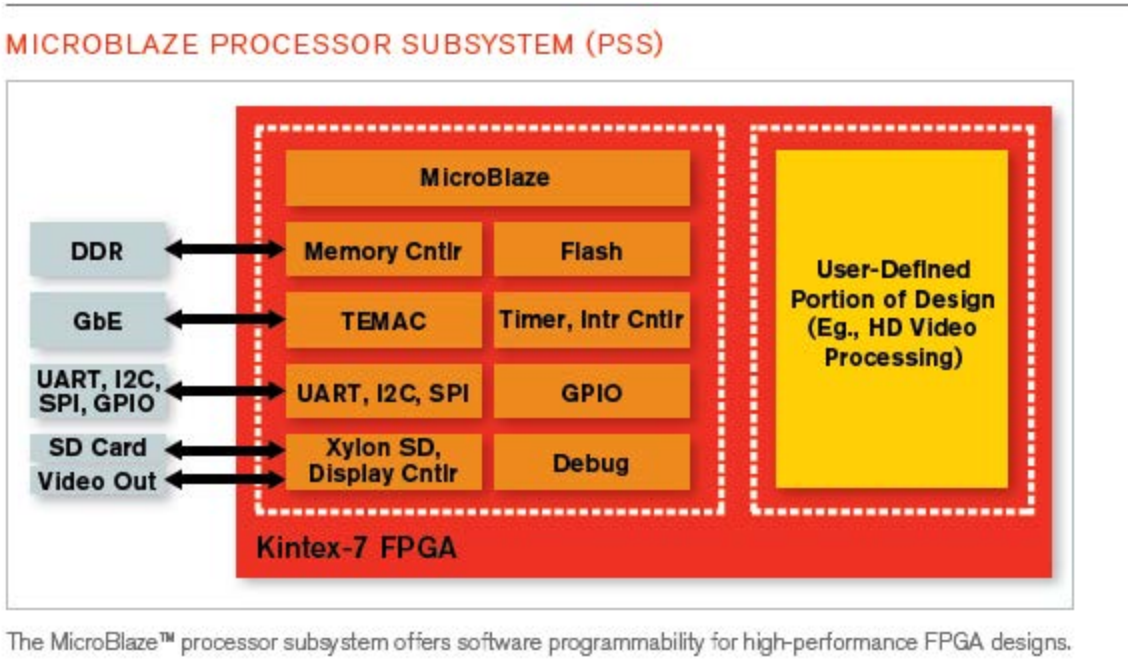
Xilinx FPGA Comparison Table

Features	Artix-7	Kintex-7	Virtex-7	Spartan-6	Virtex-6

Logic Cells	360,000	480,000	2,000,000	150,000	760,000
BlockRAM	19Mb	34Mb	68Mb	4.8Mb	38Mb
DSP Slices	1,040	1,920	3,600	180	2,016
DSP Performance (symmetric FIR)	1,306GMACs	2,845GMACs	5,335GMACs	140GMACs	2,419GMACs
Transceiver Count	16	32	96	8	72
Transceiver Speed	6.6Gb/s	12.5Gb/s	28.05Gb/s	3.2Gb/s	11.18Gb/s
Total Transceiver Bandwidth (full duplex)	211Gb/s	800Gb/s	2,784Gb/s	50Gb/s	536Gb/s
Memory Interface (DDR3)	1,066Mb/s	1,866Mb/s	1,866Mb/s	800Mb/s	1,066Mb/s
PCI Express® Interface	x4 Gen2	x8 Gen2	x8 Gen3	x1 Gen1	x8 Gen2
Agile Mixed Signal (AMS)/XADC	Yes	Yes	Yes		Yes
Configuration AES	Yes	Yes	Yes	Yes	Yes
I/O Pins	600	500	1,200	576	1,200
I/O Voltage	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.5V, 1.8V, 2.5V
EasyPath Cost Reduction Solution	-	Yes	Yes	-	Yes

Note in the above table that the Artix-7 has transceiver speed limited to < 10 Gb//s. So it does not meet one of our basic specs. It also does not have an easy path cost reduction solution. Spartan 6 also has no 10 Gb/s transceivers.

Xilinx processing capabilities provide performance and customization across a wide range of end markets including: aerospace and defense, wired and wireless communications, automotive, audio/video broadcast, industrial control, test and measurement, and consumer. Xilinx supports embedded processing by utilizing the industry-standard ARM® dual-core Cortex™-A9 MPCore™ processor in the Zynq™-7000 Extensible Processing Platform family of devices and **the MicroBlaze™ soft processor in all Xilinx FPGA devices.**



The MicroBlaze™ processor subsystem offers software programmability for high-performance FPGA designs.

1000 pc price Price info:
Virtex 6: XC6VLX75T-1FF484C (bottom of the line): < $531.00
Kintex 7: XC7K160T-1FFG676C $332.50 (non-stock at digikey)
XC7K160T-2FFG676C $398.75 (in stock at digikey)

Transceiver types:
The 7 series FPGAs GTX and GTH transceivers are power-efficient transceivers, supporting line rates from 500 Mb/s to 12.5 Gb/s for GTX transceivers and 13.1 Gb/s for GTH transceivers.

Table 1-1: **7 Series FPGAs GTX and GTH Transceiver Features**

Group	Feature	GTX	GTH
PCS	2-byte and 4-byte internal datapath to support different line rate requirements	X	X
	8B/10B encoding and decoding	X	X
	64B/66B and 64B/67B support	X	X
	Comma detection and byte and word alignment	X	X
	PRBS generator and checker	X	X
	FIFO for clock correction and channel bonding	X	X
	Programmable FPGA logic interface	X	X
	100 Gb Attachment Unit Interface (CAUI) support		X
	Native multi-lane support for buffer bypass		X
	TX Phase Interpolator PPM Controller for external voltage-controlled crystal oscillator (VCXO) replacement		X
PMA	Shared LC tank phase-locked loop (PLL) per Quad for best jitter performance	X	X
	One ring PLL per channel for best clocking flexibility	X	X
	Power-efficient adaptive linear equalizer mode called the low-power mode (LPM)	X	X
	5-tap decision feedback equalization (DFE)	X	
	7-tap DFE		X
	Reflection cancellation for enhanced backplane support		X
	TX Pre-emphasis	X	X
	Programmable TX output	X	X
	Beacon signaling for PCI Express® designs	X	X
	Out-of-band (OOB) signaling including COM signal support for Serial ATA (SATA) designs	X	X
	Line rate support up to 12.5 Gb/s	X	X
	Line rate support up to 13.1 Gb/s		X

Virtex 6:
GTX: line rates from 0.6 to 6.6 Gb/s
GTH:Support for multiple industry standards with the following line rates:

- 1.24 Gb/s to 1.397 Gb/s
- 2.48 Gb/s to 2.795 Gb/s
- 4.96 Gb/s to 5.591 Gb/s
- 9.92 Gb/s to 11.182 Gb/s